28.7 A Clock Duty-Cycle Correction and Adjustment Circuit

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In digital communication channels, the integrity of the clock signal is critical to ensuring adequate system-level performance. The clock signal must not only have the proper shape waveform and sufficient voltage amplitude, but must also have low jitter and the duty cycle must remain within a certain window. A clock signal must often span many levels of distribution before arriving at the final destination, which often distorts the duty cycle away from its ideal. In addition, some circuits perform optimally with a duty cycle offset from 50%.

In this paper we describe a clock buffer chip which provides duty-cycle correction as well as the ability to adjust the output duty cycle of the clock away from 50%. Prior analog and digital duty-cycle control implementations have either focused only on correction to a 50% duty cycle [1]-[3] or have adjusted duty cycle for relatively low-frequency applications using switched-capacitor techniques [4]. This work provides significant speed improvements over previous duty-cycle adjustment circuits in a simple and robust design, with duty cycle adjustment for clocks over 6GHz.

Figure 28.7.1 shows the top-level architecture for the clock distribution chip, which includes the duty-cycle control circuitry, support circuitry, and I/O buffers. The duty-cycle correction and adjustment method is illustrated in Fig. 28.7.2. Correction of the clock duty cycle is performed by an identical pair of specialized differential integrators. Negative feedback is provided by another integrator (referred to as the charge pump), the output of which is fed back to the correction integrators. Cascading two integrators doubles the effective gain of the loop and allows for correction of a wider range of input clock duty cycles. Adjustment of the charge pump reference allows the loop to lock to different output duty cycles.

Duty-cycle correction is performed within the integrators by adding a net positive or negative differential dc current to the integration nodes. The result is to slow one of the clock edges while speeding up its complementary edge. When this waveform is put through a differential logic buffer, the resulting clock has a new duty cycle.

Within the integrator (Fig. 28.7.3), clock rising and falling edge rates are adjusted by an additional linearized differential pair, which converts the charge pump output voltage into the differential duty-cycle control current. The core integrator has a fixed amount of pull-up and pull-down current available to counter the dc current offset. Thus, one polarity of integration is slowed while the other is sped up.

Due to the large size of the integrator PFET current sources, the parasitic capacitance on the integration nodes is quite substantial. Thus, no additional capacitance on the integration nodes is necessary at the frequencies of interest.

Diodes are used to clamp the integration nodes and keep the signal swing within specified boundaries. The diodes keep the output signal swing from saturating the HBT's of the integrator in the case where the bias current is too large for the clock frequency.

DC bias for the integrator is supplied by a 4b digital-to-analog converter (DAC). To maintain constant signal swing at the integrator output, bias current should increase linearly with frequency. The clamping diodes allow the circuit to operate across a wide frequency range without the need to adjust the DAC.

Common-mode control for the integrator outputs is accomplished by sizing the pull-up current source to be 10% larger than what is necessary to supply the current for the integrator differential pair and the duty-cycle offset differential pair. Due to the finite output impedance of the PFET current sources, the maximum signal peak for the two output nodes stays approximately 100mV below the supply and no common-mode control loop is necessary.

The differential charge pump (Fig. 28.7.4) looks much the same as the previously-mentioned integrators. The output waveform is integrated onto a 10pF MIM capacitor, giving a dc control voltage with a few millivolts of ripple. The ripple is at the same frequency as the clock signal, so no systematic clock jitter is added. When the loop is locked, the average output voltage from the charge pump is linearly proportional to the input duty cycle, with a loop gain of approximately 0.8%/mV.

Adjustment of the duty cycle away from 50% is accomplished with two PFET current sources, which source a pseudo-differential dc current into the charge-pump capacitor. These current sources are driven by a pair of 4b DACs. Controlling this differential dc current allows the user to select the output duty cycle of the loop.

The output drivers contain on-board 100Ω termination and a large $1.6V_{pp}$ differential output swing. This large swing allows the chip to drive lossy transmission lines while maintaining strong signal strength at the receiver. It is imperative that the output drivers have high bandwidth, as a clock signal which has had its duty cycle adjusted away from 50% has more upper harmonic content. Due to swing and bandwidth requirements, 2.54W of the chip's 2.8W is consumed in the ten output drivers.

Hardware testing was done on unpackaged parts using wafer probes. Testing of duty-cycle adjustment (Fig. 27.7.5) was performed with a 50% input duty cycle. The accuracy of the output duty cycle suffers above 6GHz due to output driver bandwidth limitations. Every other DAC setting has been removed for clarity.

Test equipment limitations reduce the available input duty cycle used for testing duty-cycle correction (Fig. 28.7.6) at high frequencies. The target for the output duty cycle is 50%. The integrator bias was not adjusted for frequency, giving differing loop gains. Further testing has shown the ability to correct a duty cycle of 25% at 5.75GHz, with speed again limited by the test equipment. The die micrograph is shown in Fig. 28.7.7.

Acknowledgements:
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References:

[1] Toru Ogawa and Kenji Taniguchi, "A 50% Duty Cycle Correction Circuit for PLL Output," *IEEE Int'l Symp. Circuits and Systems*, pp IV-21-IV-24, May, 2002.

[2] Jinghua Ye et al., "A 0.18μm CMOS 10-Gb/S Mulitchannel Transmitter with Duty-cycle Correction," *Proc.. 5th Int'l Conf. on ASIC*, pp 534-536, 2003.

[3] Y.C. Jang, S.J. Bae and H.J. Park, "CMOS Digital Duty Cycle Correction Circuit for Multi-Phase Clock," *Electronics Letters*, pp 1383-1384, Sept., 18, 2003.

[4] S. Karthikeyan, "Clock Duty Cycle Adjuster Circuit for Switched Capacitor Circuits," *Electronics Letters*, pp 1008–1009, Aug., 29, 2002.

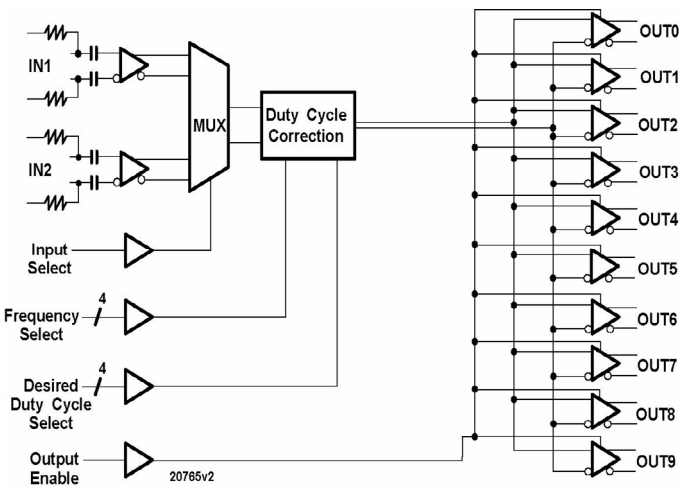

Figure 28.7.1: Chip block diagram.

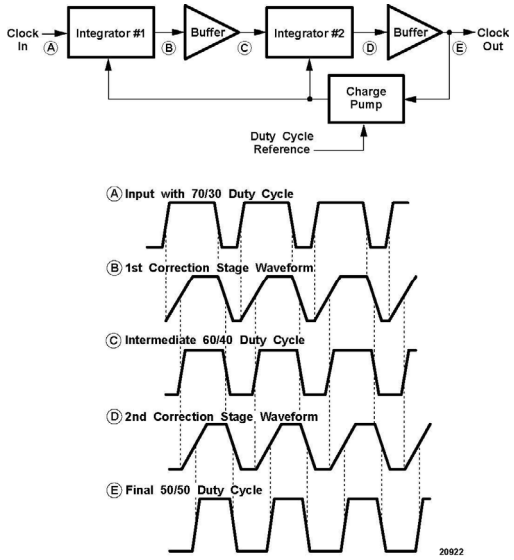

Figure 28.7.2: Duty-cycle control method.

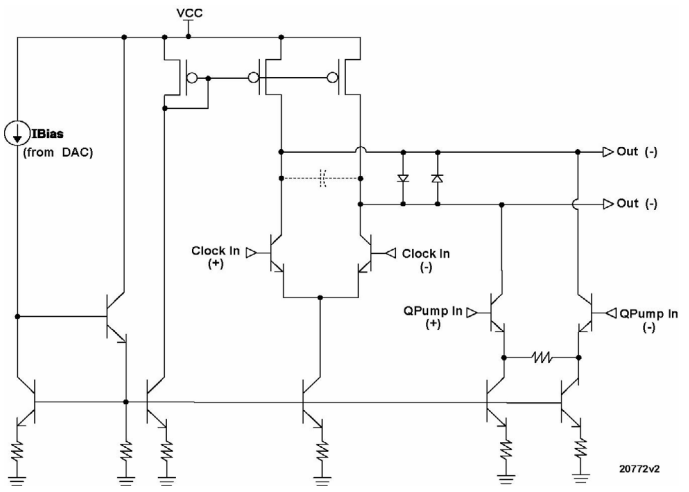

Figure 28.7.3: Integrator schematic.

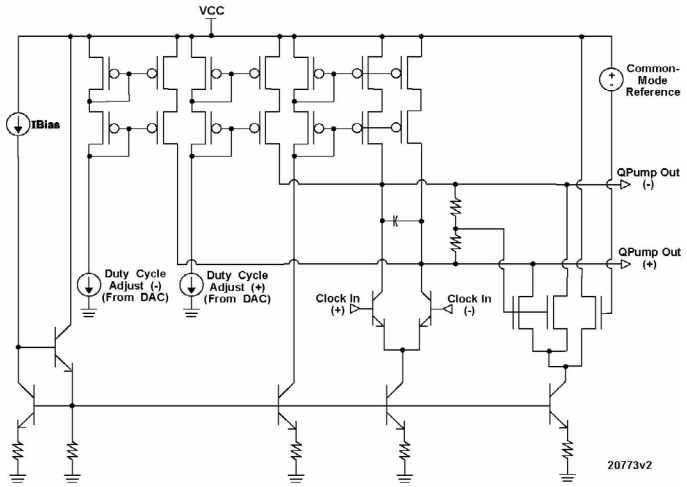

Figure 28.7.4: Charge pump schematic.

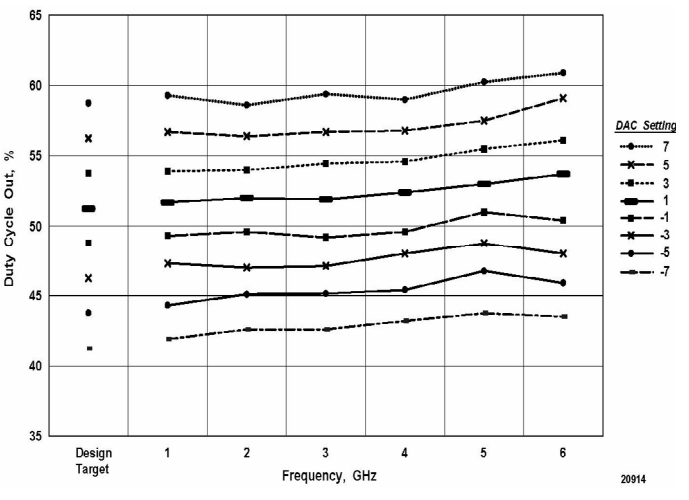

Figure 28.7.5: Measured data for duty-cycle adjustment versus frequency.

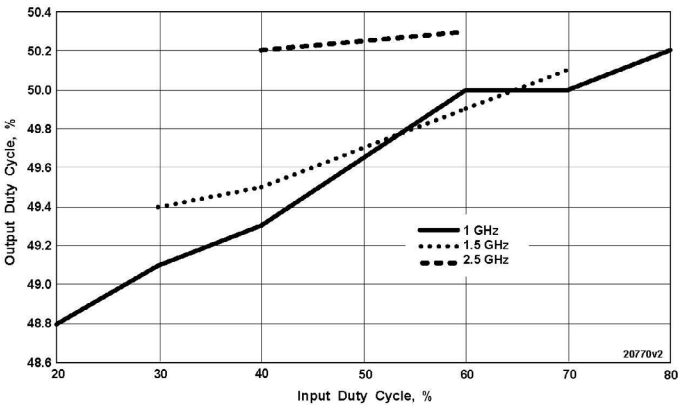

Figure 28.7.6: Measured data for duty-cycle correction.

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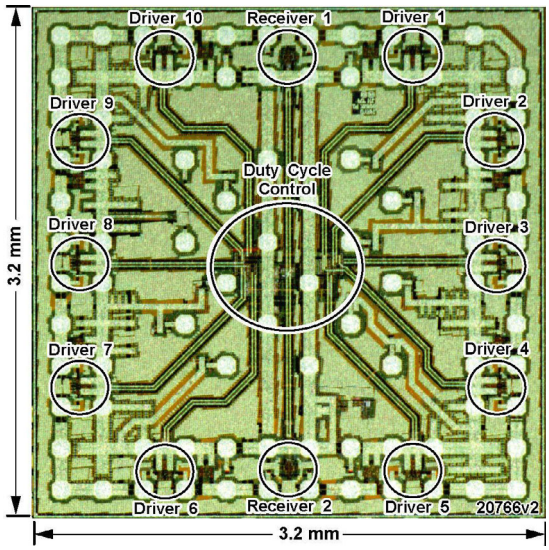

Figure 28.7.7: Die micrograph.

